Docket No.: 0756/2296

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Hisashi OHTANI et al.) Attention: Applications Branch
Serial No. 09/837,552)
Filed: April 19, 2001)
For: SEMICONDUCTOR DEVICE AND)
MANUFACTURING METHOD)
THEREOF)

RESPONSE TO NOTICE OF INCOMPLETE REPLY

AND PRELIMINARY AMENDMENT

Honorable Commissioner for Patents

Washington, D.C. 20231

Sir:

In response to the Notice of Incomplete Reply – Filing Date Granted dated October 11, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 1- 27 and add new claims 28-54 as follows:

28. A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer in only the n-channel TFT,

the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

29. A semiconductor device according to claim 28, characterized in that the first wiring line is electrically connected with the second wiring line.

30. A semiconductor device including a CMOS circuit formed by an n-channel TFT